UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/500,994	02/09/2000	Ted Johansson	032840-003	3285

21839 7590 12/26/2002

BURNS DOANE SWECKER & MATHIS L L P
POST OFFICE BOX 1404
ALEXANDRIA, VA 22313-1404

EXAMINER	
MANDALA, VICTOR A	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/500,994	Applicant(s) JOHANSSON ET AL.	
	Examiner Victor A Mandala Jr.	Art Unit 2826	

-- The MAILING DATE of this communication app ars on th cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10-22-02* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Applicant's Arguments

1. The drawings were objected to under 37 CFR 1.83(a) for not showing every feature of the claimed invention. The Applicant corrected the objection by a submission of drawing changes filed on 10-22-02. The examiner withdraws the drawing objection.

2. The Applicant has amended claims 4 and 5 around the 35 U.S.C. 112 2nd paragraph rejection. The examiner withdraws the 35 U.S.C. 112 2nd paragraph rejection on claims 4 and 5.

3. The Applicant argues the 35 U.S.C. 103 (a) rejection of U.S. Patent No. 5,240,867 Suzuki et al. in view of U.S. Patent No. 5,583,367 Blossfeld because Suzuki et al. does not state that the substrate is set to a voltage equal to ground, but Vcc. The examiner has considered the Applicant's arguments, but finds them to be unconvincing. It is understood in the art of electronics that a device operates depending only on the difference between voltages applied to the poles of the device. What is called ground is irrelevant for the voltage difference. Blossfeld also teaches in Col. 1 Lines 60-67 and Col. 2 Lines 1-2 that the use of a substrate that is grounded makes the packaging smaller by all the components on the substrate being grounded by a common ground. It can also be seen in Suzuki et al. Col. 7 Lines 56-60). The 35 U.S.C. 103 (a) rejection of U.S. Patent No. 5,240,867 Suzuki et al. in view of U.S. Patent No. 5,583,367 Blossfeld is still pending.

4. The Applicant argues the 35 U.S.C. 103 (a) rejection of U.S. Patent No. 5,240,867 Suzuki et al. in view of U.S. Patent No. 5,583,367 Blossfeld in further view of U.S. Patent No. 6,063,678 D'Anna. as being invalid due to the initial rejection of 35 U.S.C. 103 (a) rejection of U.S. Patent No. 5,240,867 Suzuki et al. in view of U.S. Patent No. 5,583,367 Blossfeld. The examiner has considered the Applicant's arguments, but finds them to be unconvincing and is explained in response to Applicant's arguments #3. The 35 U.S.C. 103 (a) rejection of U.S. Patent No. 5,240,867 Suzuki et al. in view of U.S. Patent No. 5,583,367 Blossfeld in further view of U.S. Patent No. 6,063,678 D'Anna is still pending.

Drawings

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the plug is implemented outside an area limited by a trench must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4-5, and 11-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,240,867 Suzuki et al. in view of U.S. Patent No. 5,583,367 Blossfeld.

6. Referring to claim 1, a semiconductor device arranged at a surface of a semiconductor substrate, (Suzuki et al. Figure 5 #61), having an initial doping, (Suzuki et al. Col. 6 Lines12-13), said device having an electrical connection comprising at least one plug made of a material with a high conductivity, (Suzuki et al. Figure 5 #73), between said initially doped substrate, (Suzuki et al. Figure 5 #61), and said surface of the substrate, (Suzuki et al. Figure 5 #61), said device having at least one ground connection, (Suzuki et al. Figure 5 #100), arranged to be connected to a ground pin, (Suzuki et al. Figure 6A #104), on a package, wherein said at least one ground connection, (Suzuki et al. Figure 5 #100), is arranged to be connected to said ground pin, (Suzuki et al. Figure 6A #104), using said electrical connection, (Suzuki et al. Figure 5 #100), where said substrate, (Suzuki et al. Figure 5 #61), is arranged to be connected to said ground pin, (Suzuki et al. Figure 6A #104), via a reverse side of the substrate, (Suzuki et al. Figure 5 #61), opposite said surface, and thereby being arranged to establish a connection between said ground connection, (Suzuki et al. Figure 5 #100), and said ground pin, (Suzuki et al. Figure 6A #104).

Suzuki et al. does not teach a ground pin and a ground connection but does teach a voltage source pin and connection, (Col. 7 lines 56-60). Suzuki et al. does not specify if the source voltage is a ground or a positive source voltage.

Blossfeld does teach where said substrate, (Blossfeld Figure 1 #2), is arranged to be connected to said ground pin, (Blossfeld Figure 1 #3 & Col. 2 Lines 46-48), via a reverse side of the substrate, (Blossfeld Figure 1 #2), opposite said surface, and thereby being arranged to establish a connection between said ground connection, (Blossfeld Figure 1 #3 & Col. 2 Lines 46-48), and said ground pin, (Blossfeld Figure 1 #3 & Col. 2 Lines 46-48).

It would be obvious to one skilled in the art to combine the teachings of Suzuki et al. and the teachings of Blossfeld because if a required source voltage would be ground it would be obvious to provide it to the semiconductor chip. Suzuki et al. and Blossfeld teaches the same type of substrate interconnect, but Suzuki et al. does not specificly state that the needed voltage is ground it would be obvious to apply ground through the same structure as Blossfeld teaches.

7. Referring to claim 4, a semiconductor device, (Susuki et al. Figure 5), where in said plug, (73), extends deeper into the initially doped substrate, (#61), beyond P-N junctions, (#61 & 63).

8. Referring to claim 5, a semiconductor device, (Suzuki et al. Figure5), wherein the upper end of each plug, (73), is connected to said ground connection, (79), via an electrically conductive material, (Col. 9 Line 41).

Suzuki et al. does not teach a ground connection but does teach a voltage source pin and connection, (Col. 7 lines 56-60). Suzuki et al. does not specify if the source voltage is a ground or a positive source voltage.

Blossfeld does teach where said substrate, (Blossfeld Figure 1 #2), is arranged to be connected to said ground pin, (Blossfeld Figure 1 #3 & Col. 2 Lines 46-48), via a reverse side of the substrate, (Blossfeld Figure 1 #2), opposite said surface, and thereby being arranged to establish a connection between said ground connection, (Blossfeld Figure 1 #3 & Col. 2 Lines 46-48), and said ground pin, (Blossfeld Figure 1 #3 & Col. 2 Lines 46-48).

It would be obvious to one skilled in the art to combine the teachings of Suzuki et al. and the teachings of Blossfeld because if a required source voltage would be ground it would be obvious to provide it to the semiconductor chip. Suzuki et al. and Blossfeld teaches the same type of substrate interconnect, but Suzuki et al. does not specificly state that the needed voltage is ground it would be obvious to apply ground through the same structure as Blossfeld teaches.

9. Referring to claim 11, a semiconductor integrated circuit mounted in a package, said package having a plurality of pins, (Suzuki et al. Figure 6A #107), connecting to the semiconductor circuit, (Suzuki et al. Figure 6A #60), and said circuit having a plurality of semiconductor devices, (Suzuki et al. Figure 5 #65, #68, and #67 which form a transistor and #61 and #63 which form a diode), wherein at least one of said semiconductor devices is a semiconductor device arranged at a surface of a semiconductor substrate having an initial doping, (Suzuki et al. Figure 5 #61), said device having an electrical connection comprising at least one plug made of a material with high conductivity, (Suzuki et al. Figure 5 #73), between said initially doped substrate, (Suzuki et al. Figure 5 #61), and said surface of the substrate, (Suzuki et al. Figure 5 #61), said device having at least one ground connection, (Suzuki et al. Figure 5 #100), arranged to be connected to a ground pin, (Suzuki et al. Figure 6A #104), on a package, (Suzuki et al. Figure 6A #101), wherein at least one ground connection, (Suzuki et al.

Figure 5 #100), is arranged to be connected to said ground pin, (Suzuki et al. Figure 6A #104), using said electrical connection, (Suzuki et al. Figure 5 #100), where said substrate, (Suzuki et al. Figure 5 #61), is arranged to be connected to said ground pin, (Suzuki et al. Figure 6A #104), via a reverse side of the substrate, (Suzuki et al. Figure 5 #61), opposite said surface, and thereby being arranged to establish a connection between said ground connection, (Suzuki et al. Figure 5 #100), and said ground pin, (Suzuki et al. Figure 6A #104).

Suzuki et al. does not teach a ground pin and a ground connection but does teach a voltage source pin and connection, (Col. 7 lines 56-60). Suzuki et al. does not specify if the source voltage is a ground or a positive source voltage.

Blossfeld does teach where said substrate, (Blossfeld Figure 1 #2), is arranged to be connected to said ground pin, (Blossfeld Figure 1 #3 & Col. 2 Lines 46-48), via a reverse side of the substrate, (Blossfeld Figure 1 #2), opposite said surface, and thereby being arranged to establish a connection between said ground connection, (Blossfeld Figure 1 #3 & Col. 2 Lines 46-48), and said ground pin, (Blossfeld Figure 1 #3 & Col. 2 Lines 46-48).

It would be obvious to one skilled in the art to combine the teachings of Suzuki et al. and the teachings of Blossfeld because if a required source voltage would be ground it would be obvious to provide it to the semiconductor chip. Suzuki et al. and Blossfeld teaches the same type of substrate interconnect, but Suzuki et al. does not specificly state that the needed voltage is ground it would be obvious to apply ground through the same structure as Blossfeld teaches.

10. Referring to claim 12, a semiconductor device, wherein said material has a high conductivity, (Col. 9 Line 41).

11. Referring to claim 13, a semiconductor device, wherein said material is a metal material, (Col. 9 Line 41).

12. Referring to claim 14, a semiconductor device, wherein a plurality of plugs, (#73), are provided for at least one ground connection to establish a high current connection. Suzuki et al. discloses the claimed invention except for the plurality of plugs. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a plurality of plugs, since it has been held that mere duplication of the essential working parts of the device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co. 193 USPQ8.

13. Referring to claim 15, a semiconductor device, wherein said device is a low voltage RF device, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987).

14. Referring to claim 16, a semiconductor device, wherein said plug, (#73), is implemented outside an area limited by a trench, the device having the ground connection, (Suzuki et al. Figure 5 #100), being arranged within the area.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-3 and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,240,867 Suzuki et al. in view of U.S. Patent No. 5,583,367 Blossfeld. in further view of U.S. Patent No. 6,063,678 D'Anna.

15. Referring to claim 2, a semiconductor device, wherein said material is of another type than the substrate.

Suzuki et al. does teach the substrate to be made of silicon, (Col. 9 Lines 50-55), and the plug material to be made of a polisilicon, (Col. 10 Line 38).

D'Anna also teaches the substrate to be made of silicon, (Col. 7 Line 16), and the plug material to be made of a metal or a silicide, (Figure 17 #222 & Col. 6 Lines 63-67).

It would be obvious to one skilled in the art to combine the teachings of Suzuki et al., Blossfeld, and the teachings of D'Anna because it is well known in the art that metal is a highly conductive material, which would allow a efficient electrical connection between the substrate and an electrode.

16. Referring to claim 3, a semiconductor device, wherein said at least one plug is a metal plug.

D'Anna also teaches the substrate to be made of silicon, (Col. 7 Line 16), and the plug material to be made of a metal or a silicide, (Figure 17 #222 & Col. 6 Lines 63-67).

It would be obvious to one skilled in the art to combine the teachings of Suzuki et al., Blossfeld, and the teachings of D'Anna because it is well known in the art that metal is a highly conductive material, which would allow a efficient electrical connection between the substrate and an electrode.

17. Referring to claim 6, a semiconductor device, wherein said semiconductor device is a high frequency device.

Suzuki et al. does not teach a high frequency device, but D'Anna does, (Col. 3 Lines 16-19). It would be obvious to one skilled in the art to combine the teachings of Suzuki et al., Blossfeld, and the teachings of D'Anna because the semiconductor structure allows the substrate to be used as an electrical connection, which allows the device to effectively use all of the device and allow the package to be smaller.

18. Referring to claim 7, a semiconductor device, wherein said device is a power device, (D'Anna Col. 1 Lines 20-26, and 36-39).

Suzuki et al. does not teach a power device, but D'Anna does, (Col. 1 Lines 20-26, and 36-39). It would be obvious to one skilled in the art to combine the teachings of Suzuki et al., Blossfeld, and the teachings of D'Anna because the semiconductor structure allows the substrate to be used as an electrical connection, which allows the device to effectively use all of the device and allow the package to be smaller.

19. Referring to claim 8, a semiconductor device, wherein device is a bipolar transistor and said ground connection is an emitter connection.

Suzuki et al. teaches a bipolar transistor in the claimed package. It would be obvious to one skilled in the art to combine the teachings of Suzuki et al., Blossfeld, and the teachings of D'Anna because the semiconductor structure allows the substrate to be used as an electrical connection, which allows the device to effectively use all of the device and allow the package to be smaller.

20. Referring to claim 9, a semiconductor device, wherein said transistor is a MOS transistor and said ground connection is a source connection, (D'Anna Col. 1 Lines 42- 46).

Suzuki et al. does not teach a MOS device, but D'Anna does, (D'Anna Col. 1 Lines 42-46). It would be obvious to one skilled in the art to combine the teachings of Suzuki et al., Blossfeld, and the teachings of D'Anna because the semiconductor structure allows the substrate to be used as an electrical connection, which allows the device to effectively use all of the device and allow the package to be smaller.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (703) 308-6560. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

VAMJ
December 21, 2002

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800